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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/242,822	02/24/1999	GEORGES FICHE	Q053403	1550

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EXAMINER
PHILPOTT, JUSTIN M

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 09/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/242,822	FICHE, GEORGES
	Examiner	Art Unit
	Justin M Philpott	2665

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figures 1, 4A and 4B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Regarding Figure 1, see page 1, lines 20-25 and page 6, lines 28-29 of the specification wherein applicant admits prior art.

Regarding Figures 4A and 4B, see page 10, lines 9-18 where applicant states that these figures use a prior art figure (i.e., Figure 1) incompletely. Furthermore, Figures 4A and 4B are drawn equivalent to Figure 1 with the exception that Figures 4A and 4B comprise definitive R and K values.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by applicant's cited document by Wong et al.

Regarding claim 1, Wong teaches devices for switching ATM cells (figures 1-3 – reference herein will be made specifically to figure 1) establishing a single path per virtual circuit having N.R inputs (k.n inputs) and N.R outputs (l.p outputs), N and R (k or l, and n or p) being two integers not less than two, the device comprising at least two stages, including an inlet stage (n x m stage) having R.N sets (n.k sets) of Q outputs (r) and an outlet stage (s x p stage) having R.N sets (p.l sets) of Q' inputs (r) – wherein n=p, m=n, and m=s (see page 709, col. 1, lines 4 and 17) and along the same logic k=l, thus n=m=s=p=R and k=l=N.

Furthermore, the above is characterized in that for the flow of data carried by any intermediate link (r) that is part of the single path set up between an input and an output to be a subset of the incoming flux at that input and also a subset of the outgoing flux at that output, each input of the inlet stage (n x m stage) can be connected to an output of the inlet stage which can be selected only from Q outputs (r) exclusively associated with that input; and in that each output of the outlet stage (s x p stage) can be connected to an input of the outlet stage which can be selected only from Q' inputs (r) of the output stage exclusively associated with that output.

Regarding claim 4, Wong teaches a switching device (figure 3) according to claim 1 including an inlet stage (n x m stage), a central stage (l x l' stage), and an outlet stage (m' x n' stage) characterized in that Q and Q' (r and r') are equal to R (see page 709, col. 2, line 17 and page 710, col. 1, line 10 wherein l=l' and m=m' and therefore r=r'=(Q=Q')=m=R), the central stage (l x l' stage) includes R^2 matrices (r=r', therefore the l x l' stage includes r^2 or R^2 matrices), and the matrices of the inlet stage and the matrices of the central stage are organized into R sets

(k sets, where k may be equal to r) each including N matrices (h matrices) of the inlet stage and R matrices (g matrices, where g may be equal to m) of the central stage and the matrices of the outlet stage are organized into N sets (h' sets) of R matrices (m' matrices, where m' may equal r').

Furthermore, the above is characterized in that each of the R.N matrices of the inlet stage (n x m stage) has a single input (i.e., let n=1) and R outputs (m outputs), each of the R^2 matrices of the central stage has N inputs and N outputs (l inputs and l' outputs) – the inputs being respectively connected to an output of each of the matrices of the inlet stage that belong to the same set of matrices, and each of the R.N matrices of the outlet stage (m' x n' stage) has R inputs (r' inputs) and a single output (i.e., let n'=1), those R inputs (r' inputs) being connected to outputs respectively belonging to the R sets of matrices of the central stage and of the inlet stage.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of U.S. Patent No. 5,467,347 to Petersen.

Regarding claim 2, Wong teaches the device described (see the above regarding figure 1) with the exception that Wong does not specifically disclose each matrix having exactly R.N outputs (n.k outputs) organized into R sets (n sets) of N outputs (k outputs) with each set corresponding to a respective one of the R inputs (n inputs). Rather, the device taught by Wong comprises matrices having m outputs wherein m is greater than or equal to n and wherein m does not necessarily correspond to exactly n sets of k outputs.

Petersen teaches improvements for ATM switching means wherein an inlet stage (switchport 11, see FIG. 1) is coupled to a plurality of outlet stages (switchcore 12 having planes a and b) wherein each matrix of the inlet stage (switchport 11) has outputs organized into a number of sets (one in this example) of N (n) outputs (n=2 in this example). Applying this configuration of Petersen to an ATM switching device allows for implementation on a single chip and greatly reduces hardware and maintenance costs while increasing reliability (see col. 5, lines 20-35). Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the ATM switching arrangement of Petersen to the ATM switching device of Wong in order to reduce cost and increase reliability.

Regarding claim 3, Wong teaches a switching device (figure 2) according to claim 1 including an inlet sage (n x m stage), a central stage (k x k stage), and an outlet stage (m x n stage) characterized in that, Q being equal to R (n), the inlet stage comprises N (k) matrices each having R (n) inputs each of which can be connected to an output of that matrix which can be selected only from R (m, or n wherein m=n; see page 709, col. 1, line 17) outputs of the set of outputs corresponding to that input, and the central stage (k x k) comprises a set of R (m) matrices each having N (k) inputs and N (k) outputs wherein the R (m) outputs of each set of

outputs of the inlet stage are connected to inputs belonging to the same set of R (k) matrices of the central stage.

Furthermore, the above is characterized in that, Q' being equal to R (n), the outlet stage comprises N (k) matrices each of which have R (m) inputs and R (n) outputs, wherein each output of a matrix can be connected to an input of that matrix which can be selected only from R (m) inputs corresponding to that output.

However, as with claim 2 above, Wong does not specifically disclose each matrix having inputs/outputs organized into R sets of R inputs/outputs. Rather, the device taught by Wong comprises matrices having m outputs with a single set of inputs/outputs in each matrix of each stage. Therefore, Wong does not specifically teach each matrix of the inlet stage having R^2 outputs, or R sets of R outputs, and likewise does not teach R sets of R matrices in the central stage or R^2 inputs in each matrix of the outlet stage.

As discussed above, Petersen teaches improvements for ATM switching means wherein the inlet stage (switchport 11) has R^2 outputs, or b sets of n outputs (wherein b=2 and n=2, in FIG. 1). Such an arrangement reduces cost and increases reliability and can be advantageously applied to the device taught by Wong to provide these improvements. Having R^2 outputs in the inlet stage, the device of Wong in view of the teachings of Petersen would further comprise R sets of R matrices in the central stage and similarly R^2 inputs in each matrix of the outlet stage in order to provide the desired ATM switching taught by Wong with the improvements in ATM switching taught by Petersen. Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the ATM switching teachings of Petersen to the ATM

switching device of Wong in order to provide a more robust ATM switching device with reduced cost and increased reliability.

Regarding claim 5, the device of Wong in view of Petersen teaches a switching device according to claim 3 as discussed above. Furthermore, such a device having three stages may advantageously be implemented with N and R values such that $N=2.R^2$.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,440,549 to Min et al. teaches a multi-channel, multicasting switch for an ATM network,

U.S. Patent No. 5,544,160 to Cloonan et al. teaches a terabit per second packet switch,

U.S. Patent No. 5,544,168 to Jeffrey et al. teaches an ATM switching arrangement, and

U.S. Patent No. 5,963,554 to Song teaches an ATM switch constructed from Banyan network using unit switches.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin M Philpott whose telephone number is 703.305.7357. The examiner can normally be reached on M-F, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D Vu can be reached on 703.308.6602. The fax phone numbers for the

organization where this application or proceeding is assigned are 703.872.9314 for regular communications and 703.872.9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703.305.4750.

Justin M Philpott

jmp
September 13, 2002

HUY D. VU
SUPERVISORY PATENT EXAMINER
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